AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior:

1. (Previously Presented) A method for fabricating a CMOS transistor structure, comprising the steps of:

providing a semiconductor substrate having a P-type dopant region to support an N-channel transistor of the CMOS transistor structure and an N-type dopant region to support a P-channel transistor of the CMOS transistor structure, each of the N-type dopant and P-type dopant regions having an overlying gate stack including a conductive gate;

forming lightly-doped extension regions in the semiconductor substrate adjacent each gate stack;

forming a layer of insulating material over the lightly-doped extension regions;

forming an interfacial layer of nitrogen at the interface of the insulating layer and the lightly-doped extension regions;

forming source and drain regions in the semiconductor substrate adjacent to each of the gate stacks;

forming a capping layer of contiguous silicon nitride over the semiconductor substrate and each of the gate stacks;

annealing, after the formation of the capping layer and with the capping layer in place, the extension and source and drain regions; and

removing the capping layer after the annealing.

2. (Original) The method of claim 1 wherein the extension regions for the PMOS transistors have a dopant concentration in the range of about 1-2 e20 atoms/cm3.

3. (Original) The method of claim 1 wherein the source and drain regions for the PMOS transistors have a dopant concentration in the range of about 1-2 e20 atoms/cm3.

4. (Original) The method of claim 1 wherein said interfacial nitride layer has an atomic nitrogen concentration in the range of 2-15 atomic percent.

5. (Original) The method of claim 1 wherein the insulting layer is selected from the group comprising silicon nitride and silicon oxide.

6. (Original) The method of claim 1 wherein the step of forming an interfacial layer of nitrogen is performed using one of the methods selected from the group comprising an NH_3 thermal annealing, an NH_3 or N_2 plasma treatment, or an N implantation.

7. (Original) The method of claim 1 wherein the capping layer has a thickness in the range of 200-1000 angstroms.

8. (Original) The method of claim 1 wherein the annealing step is performed in the range of 1000-1100 degrees centigrade for a time in the range of less than about 10 seconds.

9. (Original) The method of claim 1 wherein said gate stack further includes a nitride sidewall deposited with a BTBAS precursor.

10. (Previously Presented) A method for fabricating a CMOS transistor structure, comprising the steps of:

providing a semiconductor substrate having an N-type dopant region to support an PMOS transistor of the CMOS transistor structure and a P-type dopant region to support a NMOS transistor of the CMOS transistor structure, each of the N-type dopant and P-type dopant regions having an overlying gate stack including a conductive gate;

forming lightly-doped extension regions in the semiconductor substrate adjacent each gate stack, the lightly-doped extension regions in the N-type dopant region comprising a P-type dopant having a dopant concentration in the range of about 1-2 e20 atoms/cm3;

forming a layer of silicon oxide over the lightly-doped extension regions;

forming an interfacial layer of nitrogen between the lightly-doped extension regions and the silicon oxide layer, the interfacial layer of nitrogen having an

atomic nitrogen concentration in the range of 2-15 atomic percent;

forming source and drain regions in the semiconductor substrate adjacent to each of the gate stacks, the source and drain regions in the in the N-type dopant region comprising a P-type dopant having a concentration in the range of about 1-2 e20 atoms/cm3;

forming a capping layer of contiguous silicon nitride having a thickness in the range of about 200-1000 angstroms over the semiconductor substrate and each of the gate stacks;

annealing, after the formation of the capping layer and with the capping layer in place, the extension and source and drain regions at a temperature in the range of 1000-1100 degrees centigrade for a period in the range of less than about 10 seconds; and

removing the nitride cap after the annealing.

11. (Withdrawn) A semiconductor structure formed in the process of fabricating a CMOS transistor structure prior to an activating anneal, comprising:

a semiconductor substrate having an P-type dopant region to support an NMOS transistor and a N-type dopant region to support a PMOS transistor, each of the N-type dopant and P-type dopant regions having an overlying gate stack including a conductive gate;

a layer of insulating material over the semiconductor substrate and gate stack;

lightly-doped extension regions in the semiconductor substrate adjacent each gate stack;

an interfacial layer of nitrogen formed at the interface of the lighted-doped extension regions and the layer of insulating material;

source and drain regions in the semiconductor substrate adjacent to each of the gate stacks; and

a capping layer of contiguous silicon nitride over the semiconductor substrate and each of the gate stacks.

12. (Withdrawn) The structure of claim 11 wherein the layer of insulating material is silicon oxide.

13. (Withdrawn) The structure of claim 11 wherein the extension regions for the PMOS transistors have a dopant concentration in the range of about 1-2 e20 atoms/cm3.

14. (Withdrawn) The structure of claim 11 wherein the source and drain regions for the PMOS transistors have a dopant concentration in the range of about 1-2 e20 atoms/cm3.

15. (Withdrawn) The structure of claim 11 wherein the interfacial nitride layer has an atomic nitrogen concentration in the range of 2-15 atomic percent.

16. (Withdrawn) The structure of claim 11 wherein the capping layer has a thickness in the range of 200-1000 angstroms.

17. (Withdrawn) The structure of claim 11 wherein the gate stack further includes a nitride sidewall deposited with BTBAS precursor.

18. (Withdrawn) A structure formed in the fabrication of a CMOS transistor semiconductor chip prior to an activating thermal anneal, comprising:

a semiconductor substrate having a P-type dopant region to support an NMOS transistor and an N-type dopant region to support a PMOS transistor, each of the N-type dopant and P-type dopant regions having an overlying gate stack including a conductive gate supporting an oxide sidewall;

lightly-doped extension regions in the semiconductor substrate adjacent each gate stack, the lightly-doped extension regions in the N-type dopant region comprising a P-type dopant having a dopant concentration in the range of about 1-2 e20 atoms/cm3;

a layer of silicon oxide over the lightly doped extension regions;

an interfacial layer of nitrogen at the interface between the layer of silicon oxide and the lightly-doped extension regions, the interfacial layer of nitrogen having an atomic nitrogen concentration in the range of 2-15 atomic percent;

source and drain regions in the semiconductor substrate adjacent to each of the gate stacks, the source and drain regions in the N-type dopant region comprising a P-type dopant having a concentration in the range of about 1-2 e20 atoms/cm3; and

a capping layer of contiguous silicon nitride having a thickness in the range of about 200-1000 angstroms over the semiconductor substrate and each of the gate stacks.